

FIG. 1

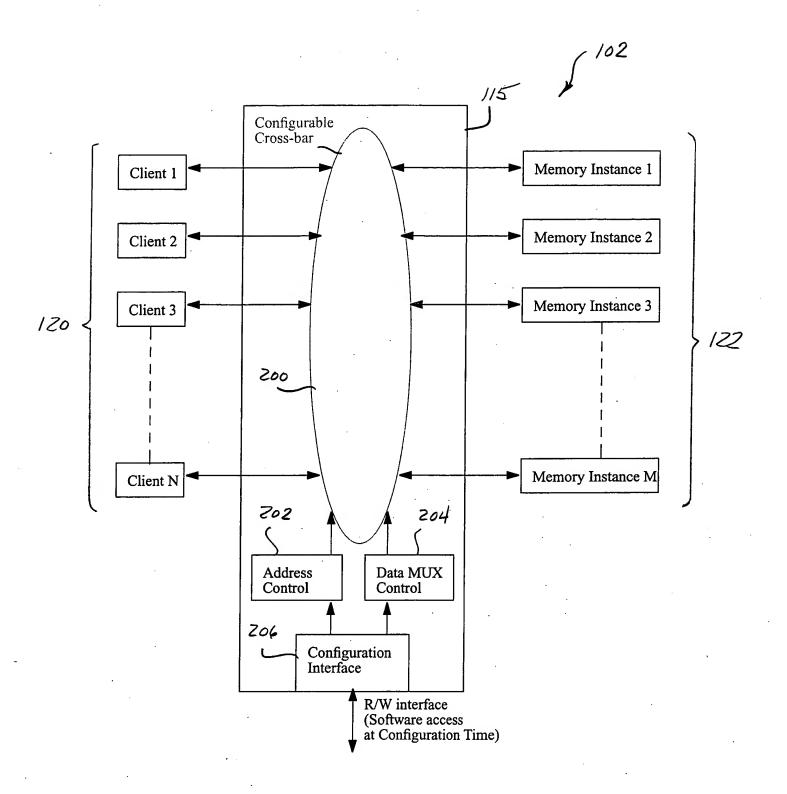
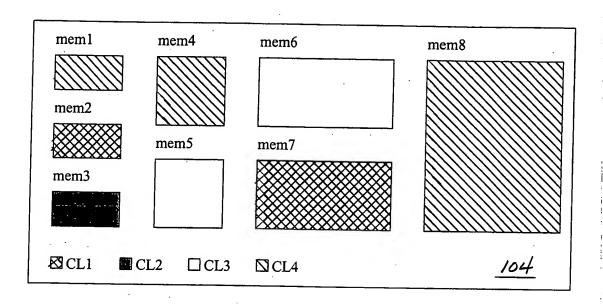


FIG. 2



716, 3A

mem1	mem4	mem6	mem8
mem2			
	mem5	mem7	
mem3			
	an all freeze		
ØCL1 ■	CL2 CL3	□ CL4	104

FIG. 3B

Memory	Configured Capacity		Idressing e [19:0]	Address Dec der Value [6:0]	Address Mask Bits [6:0]	RELEVANT BITS
Mem1	1MB	00000h	3FFFFh	7'b00x_xxxx	7'b001_1111	[19:18]
Mem2	1MB	40000h	7FFFFh	7'b01x_xxxx	7'b001_1111	[19:18]
Mem3	512KB	80000h	9FFFFh	7'b100_xxxx	7'b000_1111	[19:17]
Mem4	512KB	A0000h	BFFFFh	7'b101_xxxx	7'b000_1111	[19:17]
Mem5	256KB	C0000h	CFFFFh	7'b110_0xxx	7'b000_0111	[19:16]
Mem6	128KB	D0000h	D7FFFh	7'b110_10xx	7'b000_0011	[19:15]
Mem7	128KB	D8000h	DFFFFh	7'b110_11xx	7'b000_0011	[19:15]
Mem8	64KB	E0000h	E3FFFh	7'b111_000x	7'b000_0001	[19:14]
Mem9	32KB	E4000h	E5FFFh	7'b111_0010	7'b000_0000	[19:13]

F16, 4A

Memory Size	Mask bits [6:0]		
1MB	7'b001_1111		
512KB	7'b000_1111		
256KB	7'b000_0111		
128KB	7'b000_0011		
64KB	7'b000_0001		
32KB	7'b000_0000		

FIG. 4B

No. Of Bits	Description		
[6:0]	Address DecoderValue for a particular internal memory. Instance.		
[6:0]	Address Mask Value as mentioned in the above table, depending on the memory instance size.		
[4:0]	Master client for the memory instance. "00001" for CL1 "10100" for CL20.		

FIG. 4C

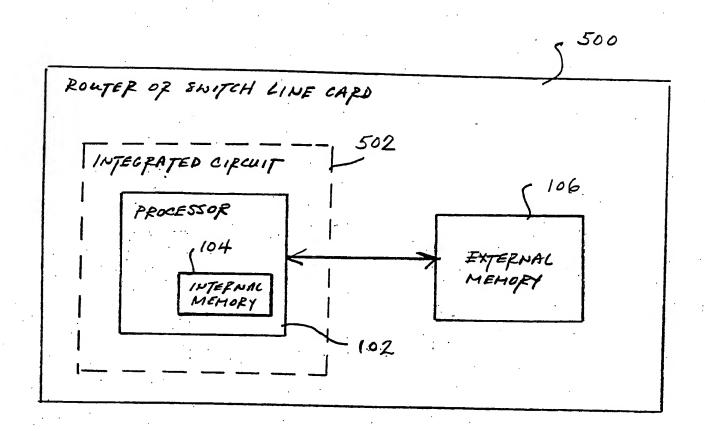


FIG. 5